bq24740/1EVM (HPA206) For Multicell Synchronous Notebook Charger

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1 Introduction

1.1 EVM Features

- Evaluation module for bq24740/1
- High-efficiency NMOS-NMOS synchronous buck charger with 300-kHz frequency
- Battery/adapter to system power selector function
- User-selectable 2-cell, 3-cell, or 4-cell Li-ion battery voltage
- User-programmable battery regulation voltage with external voltage source (4.2/cell by default)
- User-programmable charge current with external voltage source (3 A by default)
- User-programmable input current limit with external voltage source (4.5 A for bq24740, 4 A for bq24741 by default)
- Pin-programmable interface for control and status communications with host
- AC adapter operating range 18 V to 22 V
- LED indication for control and status signals
- Test points for key signals available for testing purpose. Easy probe hook-up
- Jumpers available. Easy to change connections

1.2 General Description

The bq24740/1 evaluation module is a complete charger module for evaluating a multicell synchronous notebook charge and path selection solution using the bq24740/1 devices. It is designed to deliver up to 6 A of charge current to Li-ion or Li-polymer applications. The charge current is programmable by external voltage input.

The bq24740/1 has a highly integrated battery charge controller designed to work with external host commands. The battery voltage, charge current, input current limit, and other system parameters are pin programmable.

The dynamic power management (DPM) function modifies the charge current depending on system load conditions, avoiding ac adapter overload.

High-accuracy current sense amplifiers enable accurate measurement of the ac adapter current, allowing monitoring of overall system power.

For details, see the bq24740 data sheet (SLUS736), and the bq24741 data sheet (SLUS875).

1.3 I/O Description

Jack		Description
J1–ACPWR		AC adapter, positive output
J1–PGND		AC adapter, negative output
J2–1	} BYPASS } BYPASS_EX	BYPASS drive signal on EVM
J2–2		Gate of Q2
J2–3		External BYPASS drive signal
J3–1	} ACDRV } ACDRV_EX	ACDRV drive signal on EVM
J3–2		Gate of Q1
J3–3		External ACDRV drive signal
J4–BYPASS_EX		External BYPASS drive signal
J4–ACDRV_EX		External ACDRV drive signal
J4–GND		Ground
J5–1	} BATDRV_EX } BATDRV	External ACDRV drive signal
J5–2		Gate of Q3
J5–3		ACDRV drive signal on EVM
J6–VREF		IC REFERENCE VOLTAGE vref
J6–VDAC		VDAC pin
J6–VDACEXT		External VDAC voltage
J6–GND		Ground
J7–PULLUP		Pullup voltage source
J7–LEDPWR		LED pullup power line
J8–$\overline{\text{EXTPWR}}$		$\overline{\text{EXTPWR}}$ pin
J8–GND		Ground
J8–BAT		Connected to battery pack
J8–SYS		Connected to system
J9–1	} 4.2V REG	REGN pin
J9–2		VADJ pin
J10–VEXT		External power supply, positive output
J10–GND		External power supply, negative output
J11–$\overline{\text{CHGEN}}$		$\overline{\text{CHGEN}}$ pin for bq24740, CE pin for bq24741
J11–$\overline{\text{IADSLP}}$		$\overline{\text{IADSLP}}$ pin or bq24740, TRICKLE pin for bq24741
J11–CELLS		CELLS pin
J12–VADJ		VADJ pin

Jack	Description
J12–ACSET	ACSET pin
J12–SRSET	SRSET pin
J13–VPULUP	Pullup voltage source
J13–CELLS	CELLS pin output
J13–GND	Ground
J14–$\overline{\text{LOPWRMODE}}$	LPMD pin for bq24740, $\overline{\text{LPMOD}}$ pin for bq24741.
J14–IADPTF	R25 terminal connected to C18
J14–VREF	IC reference voltage VREF
J14–$\overline{\text{DPMDET}}$	$\overline{\text{DPMDET}}$ pin
J15–BYPASS	BYPASS pin
J15–LED	LED drive
J16–EXT BATDRV	External BATDRV drive signal
J16–GND	Ground
J17–ACDRV	ACDRV pin
J17–LED	LED drive
J18–BATDRV	BATDRV pin
J18–LED	LED drive
J19–VPULUP	Pullup voltage source
J19–$\overline{\text{IADSLP}}$	$\overline{\text{IADSLP}}$ pin output for bq24740, TRICKLE pin output for bq24741
J20–VPULUP	Pullup voltage source
J20–$\overline{\text{CHGEN}}$	$\overline{\text{CHGEN}}$ pin output for bq24740, CE pin output for bq24741
J21–VREF	IC reference voltage VREF
J21–VDAC	VDAC pin (#11)
J21–VDACEXT	External VDAC voltage

1.4 Control and Key Parameters Setting

Jack	Description	Factory Setting
J2	BYPASS drive setting 1-2: Use onboard BYPASS drive 2-3: Use external BYPASS drive	Jumper on 1-2
J3	ACDRV drive setting 1-2: Use onboard ACDRV drive 2-3: Use external ACDRV drive	Jumper on 1-2
J5	BATRDRV drive setting 1-2: Use External BARDRV drive 2-3: Use onboard BATDRV drive	Jumper on 2-3
J7	The pullup power source supplies the LEDs when on. LED has no power source when off.	Jumper On
J9	Connect REGN to VADJ when on	Jumper Off
J13	Number of cells selection 1-2 (PULLUP-CELLS) : 4 cells 2-3 (GND-LO) : 3 cells Open: 2 cells	Jumper on 2-3 (3 cells)
J15	The conduction of the BYPASS MOSFET is indicated by LED when on.	Jumper On
J17	The conduction of the AC MOSFET is indicated by LED when on.	Jumper On
J18	The conduction of the battery MOSFET is indicated by LED when on.	Jumper On
J19	$\overline{\text{IADSLP}}$ pulled to high when on for bq24740, TRICKLE pulled to high when on for bq24741	Jumper Off

Jack	Description	Factory Setting
J20	Disable charge process when on for bq24740, enable charge process when on for bq24741	Jumper On for bq24740, Off for bq24741
J21	VDAC voltage source setting 1-2 : Connect VREF to VDAC 2-3 : Connect external voltage source to VDAC	Jumper on 1-2 (VREF and VDAC)

1.5 Recommended Operating Conditions

SYMBOL		DESCRIPTION	MIN	TYP	MAX	UNIT	Notes
V_{IN}	Supply voltage	Input voltage from ac adapter input	18	19	22	V	
V_{BAT}	Battery voltage	Voltage applied at VBAT terminal of J8	6	7–16.8	20	V	
I_{AC}	Supply current	Maximum input current from ac adapter input	0		4.5	A	
I_{chrg}	Charge current	Battery charge current	2	3 or 4	6	A	
T_J	Operating junction temperature range		0		125	°C	

2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA206 evaluation board. On the test procedure the following naming conventions are followed. See the HPA206 schematic for details.

VXXX :	External voltage supply name (VADP, VBT, VSBT)
LOADW:	External load name (LOADR, LOADI)
V(TPyyy):	Voltage at HPA206 internal test point TPyyy. For example, V(TP12) means the voltage at TP12.
V(Jxx):	Voltage at HPA206 jack terminal Jxx.
V(TP(XXX)):	Voltage at test point *XXX*. For example, V(ACDET) means the voltage at the test point which is marked as *ACDET*.
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON :	HPA206 internal jumper Jxx terminals are shorted
Jxx OFF:	HPA206 internal jumper Jxx terminals are open
Jxx (-YY-) ON:	HPA206 internal jumper Jxx adjacent terminals marked as *YY* are shorted
Measure: → A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	A,B Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components.

2.2 Equipment

2.2.1 Power Supplies

Power supply #1 (PS#1): a power supply capable of supplying 20 V at 5 A is required.
Power supply #2 (PS#2): a power supply capable of supplying 5 V at 1 A is required.
Power supply #3 (PS#3): a power supply capable of supplying 20 V at 1 A is required.

2.2.2 Load #1

A 30-V (or above), 5-A (or above) electronic load that can operate at constant current mode

2.2.3 Load #2

A HP 6060B 3- to 60-V/0-to 60-A, 300-W system DC electronic load or equivalent

2.2.4 Meters

Seven Fluke 75 multimeters, (equivalent or better)
or four equivalent voltage meters and three equivalent current meters.

The current meters must be capable of measuring a 5-A+ current.

2.3 Equipment Setup

A. Set the power supply #1 for 0 V ± 100 mVDC, 5 V ± 0.1-A current limit and then turn off supply.
B. Connect the output of power supply #1 in series with a current meter (multimeter) to J1 (ACPWR, GND).
C. Connect a voltage meter across J1 (ACPWR, GND).
D. Set the power supply #2 for 3.3 V ±100 mVDC, 1 ±0.1-A current limit and then disable the output.
E. Set the power supply #3 for 10.5 V ±100 mVDC, 1 ±0.1-A current limit and then disable the output.
F. Connect the output of power supply #2 to J10 (VEXT, GND).
G. Turn off Load #1.
H. Turn off Load #2.
I. Connect a voltage meter across J8 (BAT, GND).
J. Connect a voltage meter across J8 (SYS, GND).
K. J2 (BYPASS): ON, J3 (ACDRV): ON, J5 (BATDRV): ON, J7: ON, J21 (VREF, VDAC): ON, J9: OFF, J19: OFF, J13 (CELLS, GND): ON, J15: ON, J17: ON, J18: ON. J20: ON (for bq24740 only), OFF (For bq24741 only).

After the preceding steps, the test setup for HPA206 (bq24740EVM) is shown in Figure 1.

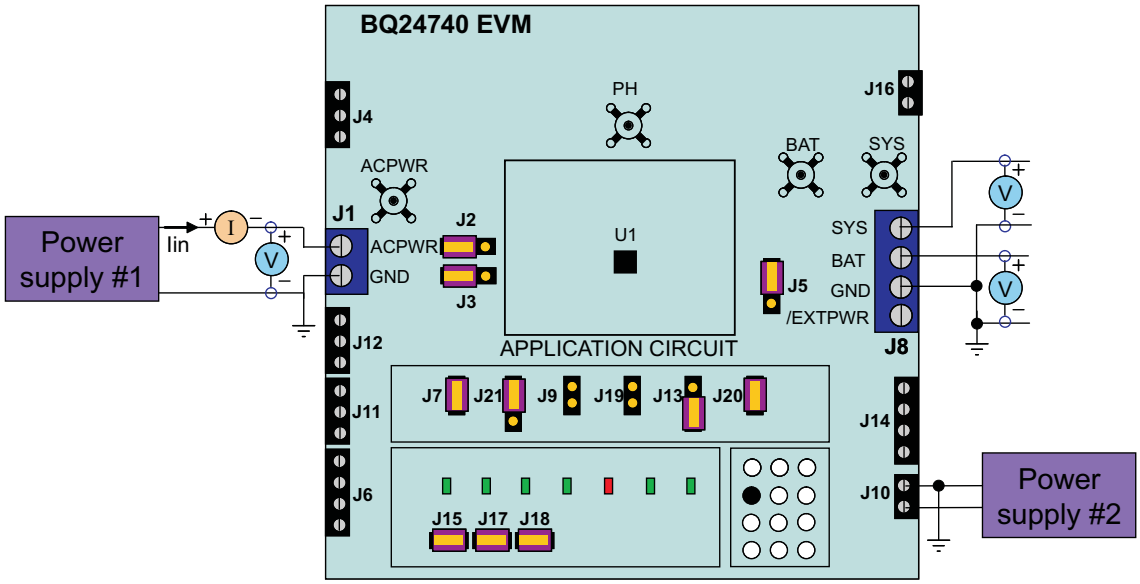


Figure 1. Original Test Setup for HPA206 (bq24740EVM)

2.4 Procedure

2.4.1 AC Adapter Detection Threshold

1. Make sure the Equipment Setup steps of the previous section are followed.
2. Enable the output of PS#2.
3. Turn on PS#1.
   Measure → V(J8(VSYS)) = 0 ±500 mV
   Measure → V(TP(VREF)) = 0 ±1 V
   Measure → V(TP(REGN)) = 0 V ±500 mV
4. Increase the output voltage of PS#1 until D7 ($\overline{\text{EXTPWR}}$) is on, but do not exceed 20 V.
   Measure → V(TP(ACDET)) = 2.4 V ±200 mV
   Measure → V(J1(POS)) = 17.9 V ±1 V
   Measure → V(J8(SYS)) = 17.9 V ±1 V
   Measure → V(TP(VREF)) = 3.3 V ±200 mV
   Measure → D2 ($\overline{\text{BYPASS}}$) on. D3 (ACDRV) on.
   Observe → D5 ($\overline{\text{CHGEN}}$) off (for bq24740 only), D5 (CE) on (for bq24741 only).

2.4.2 Selection of Regulation Voltage

1. Increase the voltage of PS#1 until V(J1(POS)) = 19 V ±0.1 V.
   Measure → V(J8(BAT, GND)) = 0 V ±2 V
   Uninstall J20 enable the charging (for bq24740 only)
   Observe → D5 ($\overline{\text{CHGEN}}$) on
   Install J20 enable the charging (for bq24741 only)
   Observe → D5 (CE) off
   Measure → V(TP(REGN)) = 6 V ±500 mV
   Measure → V(J8(BAT)) = 12.6 V ±200 mV
2. Install J13 (CELLS, VPULUP)
   Measure → V(J8(BAT)) = 16.8 V ±200 mV
3. Install J13(CELLS, GND)
   Measure → V(J8(BAT)) = 12.6 V ±200 mV

2.4.3 Charge Current and AC Current Regulation (DPM)

1. Install J20 disable the charging (for bq24740 only). Uninstall J20 disable the charging (for bq24741 only).
2. Connect the Load #2 in series with a current meter (multimeter) to J8 (BAT, GND). Ensure that a voltage meter is connected across J8 (BAT, GND). Turn on the Load #2. Use the constant voltage mode. Set the output voltage to 10.5 V.
3. Connect the output of the Load #1 in series with a current meter (multimeter) to J8 (SYS, GND). Ensure that a voltage meter is connected across J8 (SYS, GND). Turn on the power of the Load #1. Set the load current to 4 A ±50 mA (for bq24740 only) or 3.4A ±50mA (for bq24741 only), but disable the output. The setup is now like Figure 2 for HPA206. Ensure that Ibat = 0 A ±10 mA and Isys = 0 A ±10 mA.

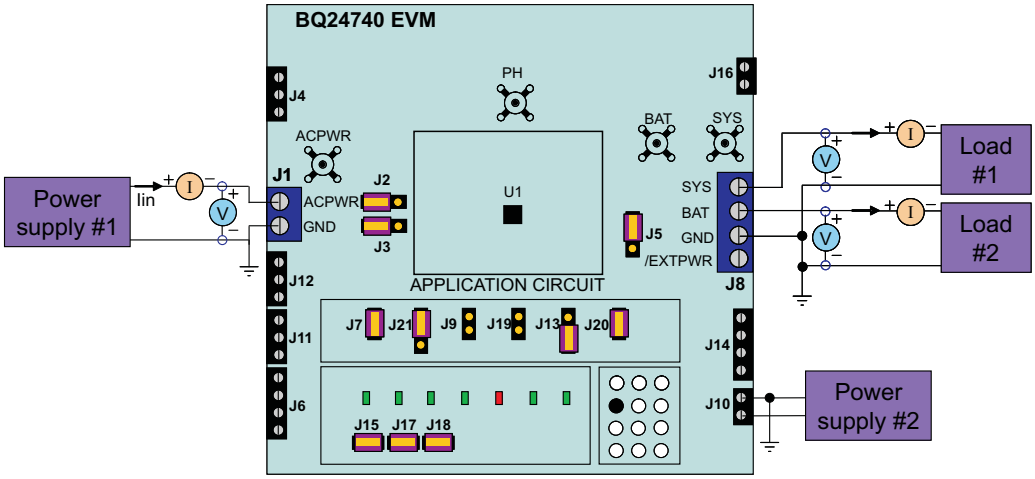


Figure 2. Test Setup for HPA206 (bq24740EVM)

4. Uninstall J20 Enable the charging (for bq24740 only).
   Observe → D5 (CHGEN) on
   Install J20 Enable the charging (for bq24741 only).
   Observe → D5 (CE) off.
5. Measure → Ibat = 3000 mA ±200 mA
6. Enable the output of the Load #1.
   Observe → D6 (DPMDET) on
   Measure → Isys = 4000 mA ±200 mA, Ibat = 1000 mA ±500 mA, Iin = 4500 mA ±400 mA (for bq24740 only)
   Measure → Isys = 3400 mA ±200mA, Ibat = 1000 mA ±500 mA, Iin = 4000 mA ±400 mA (for bq24741 only)
7. Turn off the Load #1.
   Measure → Isys = 0 ±100 mA, Ibat = 3000 mA ±200 mA

2.4.4 Power Path Selection

1. Install J20. (Disable the charging) (for bq24740 only).
   Observe → D5 (CHGEN) off.
   Uninstall J20 disable the charging (for bq24741 only)
   Observe → D5 (CE) on
2. Replace Load #2 and current meter with PS#3. Ensure that a voltage meter is connected across J8 (BAT, GND). Enable the output of the PS #3. Ensure that the output voltage is 10.5 V±500 mV.
3. *Measure* → V(J8(SYS)) = 19 V ±1 V (adapter connected to system)
   Observe → D2(BYPASS) on, D3 (ACDRV) on, D4 (BATDRV) off
4. Turn off PS#1.
   Measure → V(J8(SYS)) = 10.5 V ±1 V (battery connected to system)
5. *Observe* → D2(BYPASS) off, D3 (ACDRV off, D4 (BATDRV) on.

3 PCB Layout Guideline

1. It is critical that the exposed power pad on the backside of the bq24740/1 package be soldered to the PCB ground. Ensure that sufficient thermal vias are right underneath the IC, connecting to the ground plane on the other layers.
2. Route the control stage and the power stage separately. At each layer, the signal ground and the power ground are connected only at the power pad.
3. AC current sense resistor must be connected to ACP and ACN with a Kelvin contact. Minimize the area of this loop. Place the decoupling capacitors for these pins as close to the IC as possible.
4. Connect the charge current sense resistor to SRP, SRN with a Kelvin contact. Minimize the area of this loop. Place the decoupling capacitors for these pins as close to the IC as possible.
5. Place the decoupling capacitors for PVCC, VREF, REGN underneath the IC (on the bottom layer), and make the interconnections to the IC as short as possible.
6. Place the decoupling capacitors for BAT, IADAPT close to the corresponding IC pins, and make the interconnections to the IC as short as possible.
7. Decoupling capacitor(s) for the charger input must be placed close to Q4 drain and Q5 source.

4 Bill of Materials, Board Layout, and Schematics

4.1 Bill of Materials

bq24740 -001	bq24741 -002	RefDes	Value	Description	Size	Part Number	MFR
0	0	C1, C3, C11, C18	Open	Capacitor, Ceramic	0805	STD	STD
0	0	C12, C25	Open	Capacitor, Ceramic	1206	STD	STD
2	2	C13, C32	10uF	Capacitor, Ceramic, 25V, X5R, 10%	1206	STD	STD
4	4	C14, C15, C28, C29	10uF	Capacitor, Ceramic, 25V, X5R, 10%	1210	GRM32DR61E106K A12L	Murata
1	1	C19	2.2uF	Capacitor, Ceramic, 25V, X5R, 10%	1210	STD	STD
5	5	C2, C7, C10, C16, C27	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0805	STD	STD
2	2	C22, C23	10nF	Capacitor, Ceramic, 50V, X7R, 10%	0603	STD	STD
0	0	C24	Open	Capacitor, Ceramic	1210	STD	STD
0	0	C31	Open	Capacitor, Ceramic	1210	STD	STD
1	1	C4	1uF	Capacitor, Ceramic, 25V, X5R, 10%	0603	GRM188R61E105K A12D	muRata
1	1	C5	100pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	STD	STD
3	3	C6, C8, C27	1uF	Capacitor, Ceramic, 25V, X5R, 10%	0805	GRM216R61E105K A12D	muRata
8	8	C9, C17, C20, C21, C26, C30, C33, C34	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	STD	STD
1	1	D1	BAT54	Diode, Schottky, 200-mA, 30-V	SOT23	BAT54	Vishay-Liteon
6	6	D2, D3, D4, D5, D7, D8	160-1183-1-ND	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	0603	160-1183-1-ND	Lite On
1	1	D6	160-1181-1-ND	Diode, LED, Red, 1.8-V, 20-mA, 20-mcd	0603	160-1181-1-ND	Lite On
1	1	D9	MBRS130TR	Diode, Schottky, 1A, 30V	SMB	MBRS130TR	IR
1	1	J1	D120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	D120/2DS	OST

2	2	J10, J16	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
5	5	J2, J3, J5, J13, J21	PTC36SAAN	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 inch x 3	PTC36SAAN	Sullins
3	3	J4, J11, J12	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
2	2	J6, J14	ED555/4DS	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25 inch	ED555/4DS	OST
7	7	J7, J9, J15, J17, J18, J19, J20	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
1	1	J8	D120/4DS	Terminal Block, 4-pin, 15-A, 5.1mm	0.80 x 0.35 inch	D120/4DS	OST
1	0	L1	8.2uH	Inductor, SMT, 16A, 24.8milliohm	0.51 x 0.51 inch	IHLP5050CE8R2M01	Vishay
0	1	L1	10uH	Inductor, SMT, 16A, 24.8milliohm	0.51 x 0.51 inch	IHLP5050CE10RM01	Vishay
3	3	Q1, Q2, Q3	Si4435DY	MOSFET, P-ch, 30-V, 8.0-A, 20-milliohm	SO8	Si4435DY	Siliconix
3	3	Q12, Q14, Q16	TP0610K	Mosfet, P-Ch, 60V, Rds 6 ohms, Id 185 mA	SOT-23	TP0610K	Vishay-Siliconix
2	2	Q4, Q5	FDS6680A	Transistor, MOSFET, NChan, 30V, 12.5A, Rds 9.5 milliohm	SO8	FDS6680A	Fairchild
12	12	Q6, Q7, Q10, Q13, Q15, Q17, Q18, Q19, Q20, Q21, Q22, Q23	2N7002DICT	MOSFET, N-ch, 60-V, 115-mA, 1.2-Ohms	SOT23	2N7002DICT	Vishay-Liteon
3	3	Q8, Q9, Q11	NDS0605	MOSFET,P-ch, -60 V, 180-mA, 5 Ohms	SOT-23	NDS0605	Vishay
1	1	R1	430K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	2	R10, R50	4	Anti-surge Resistor, Chip, 1/2W, 5%	1210	ERJ-P14J4R0U	Panasonic - ECG
8	8	R11, R3, R4, R18, R19, R22, R44, R48	10K	Resistor, Chip, 1/16W, 1%	0402	STD	STD
1	1	R12	0.01	Resistor, Chip, 1/2W, 1%	2010	STD	STD
1	0	R13	0.01	Resistor, Chip, 1/2W, 1%	2010	STD	STD
0	1	R13	0.02	Resistor, Chip, 1/2W, 1%	2010	STD	STD
2	2	R14, R15	10K	Resistor, Chip, 1/16W, 5%	0603	STD	STD
3	3	R16, R45, R49	100K	Resistor, Chip, 1/10W, 0.1%	0805	STD	STD
1	1	R2	66.5K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
12	12	R20, R5, R17, R21, R23, R26, R28, R29, R31, R32, R34, R35	100K	Resistor, Chip, 1/16W, 5%	0402	STD	STD
1	1	R24	68K	Resistor, Chip, 1/10W, 0.1%	0805	STD	STD
2	2	R25, R43	0 ohm	Resistor, Chip, 1/16W, 5%	0402	STD	STD
1	0	R27	43K	Resistor, Chip, 1/10W, 0.1%	0805	STD	STD
0	1	R27	150K	Resistor, Chip, 1/10W, 0.1%	0805	STD	STD
7	7	R30, R33, R36, R38, R39, R41, R42	2.2K	Resistor, Chip, 1/16W, 5%	0603	STD	STD
3	3	R37, R40, R47	20K	Resistor, Chip, 1/16W, 5%	0603	STD	STD
1	0	R46	82K	Resistor, Chip, 1/10W, 0.1%	0805	STD	STD
0	1	R46	66.5K	Resistor, Chip, 1/10W, 0.1%	0805	STD	STD

1	0	R6	30K	Resistor, Chip, 1/16W, 1%	0402	STD	STD
0	1	R6	97.6K	Resistor, Chip, 1/16W, 1%	0402	STD	STD
1	1	R7	200K	Resistor, Chip, 1/16W, 1%	0402	STD	STD
1	0	R8	49.9K	Resistor, Chip, 1/16W, 1%	0402	STD	STD
0	1	R8	73.2K	Resistor, Chip, 1/16W, 1%	0402	STD	STD
1	0	R9	1.4M	Resistor, Chip, 1/16W, 1%	0402	STD	STD
12	12	SJ1,SJ2,SJ3 ,SJ4,SJ5,SJ 6,SJ7,SJ8,S J9,SJ10,SJ1 1,SJ12	929950-00	Shorting jumpers, 2-pin, 100mil spacing,		929950-00	3M/ESD
4	4			6-32 NYL nuts			
4	4	ST1,ST2,ST 3,ST4	4816	STANDOFF M/F HEX 6-32 NYL .500"	sf_thvt_325_rnd	4816	Keystone
4	4	TP1, TP2, TP27, TP28	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	0.200 inch	131-4244-00	Tektronix
11	11	TP4, TP5, TP7, TP8, TP9, TP10, TP13, TP15, TP16, TP17, TP18	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
2	2	TP6, TP26	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	0	U1	BQ24740RH D	IC, Battery Charge Controller/Selector w/DPM	QFN-28	BQ24740RHD	TI
0	1	U1	BQ24741RH D	IC, Battery Charge Controller/Selector w/DPM	QFN-28	BQ24741RHD	TI
1	1	--	HPA206	PCB, 4 In × 4 In × 0.062 In		PCB	Any

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.2 Board Layout

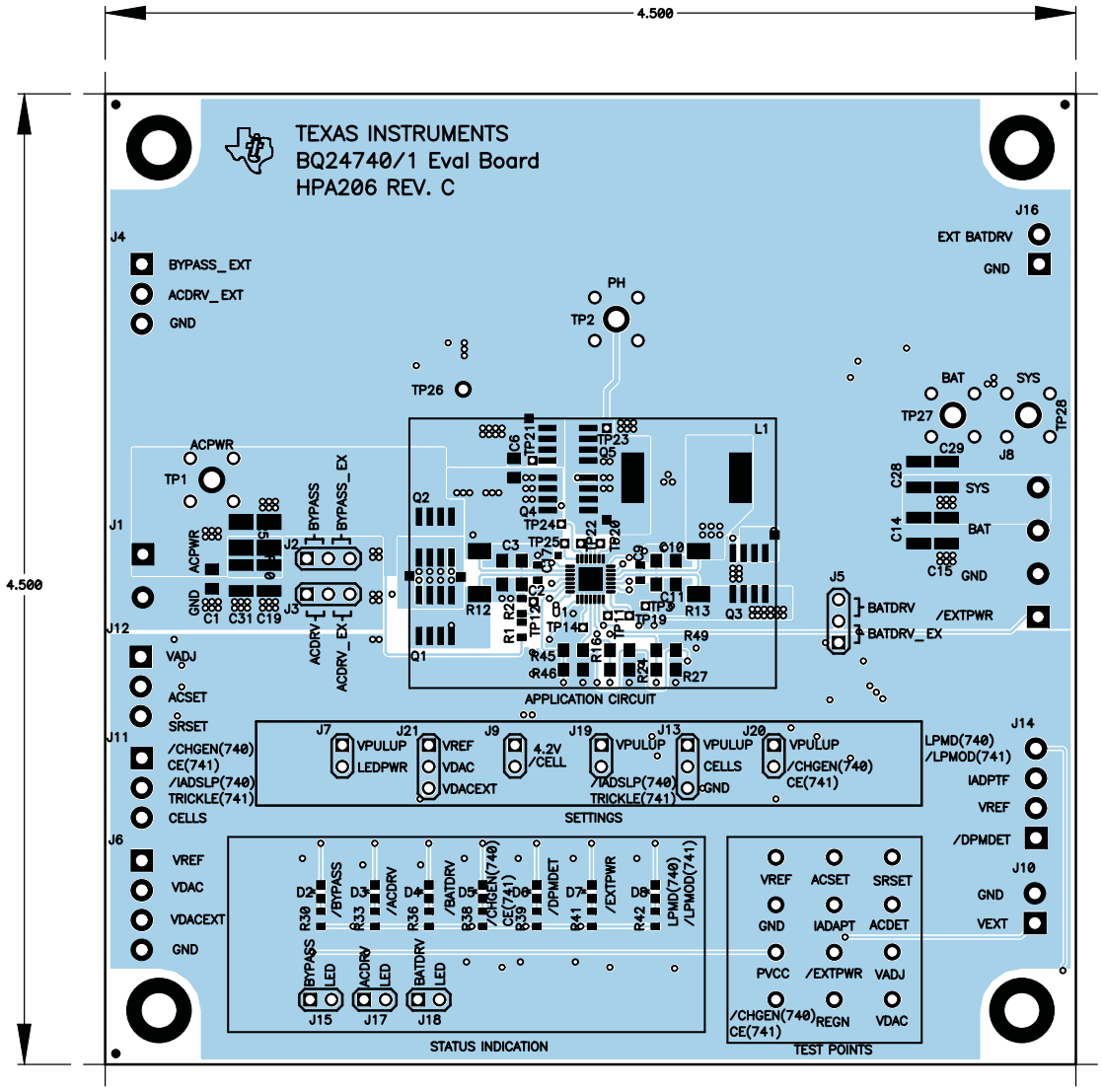


Figure 3. Top and Silk Layer

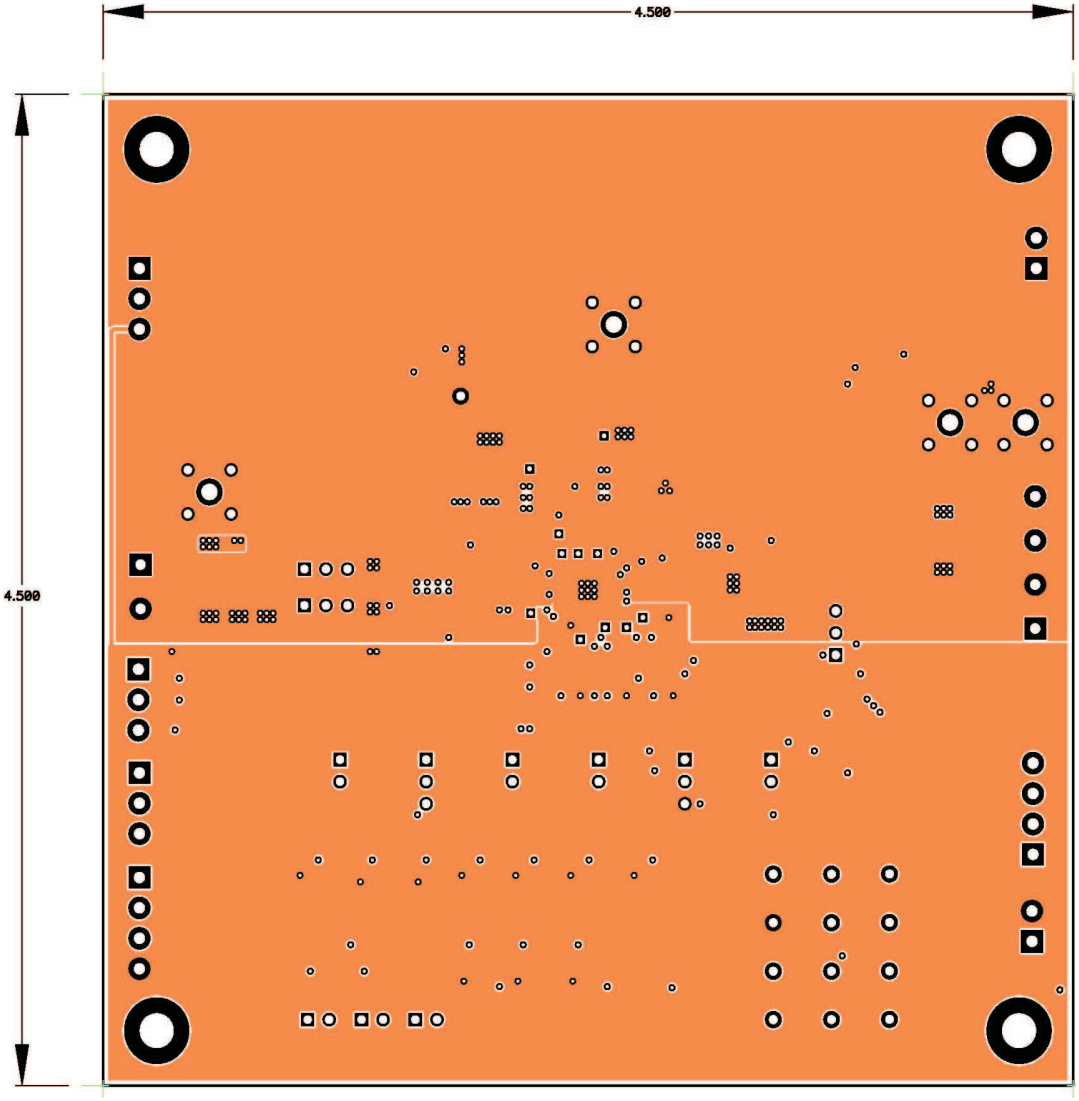


Figure 4. Second Layer

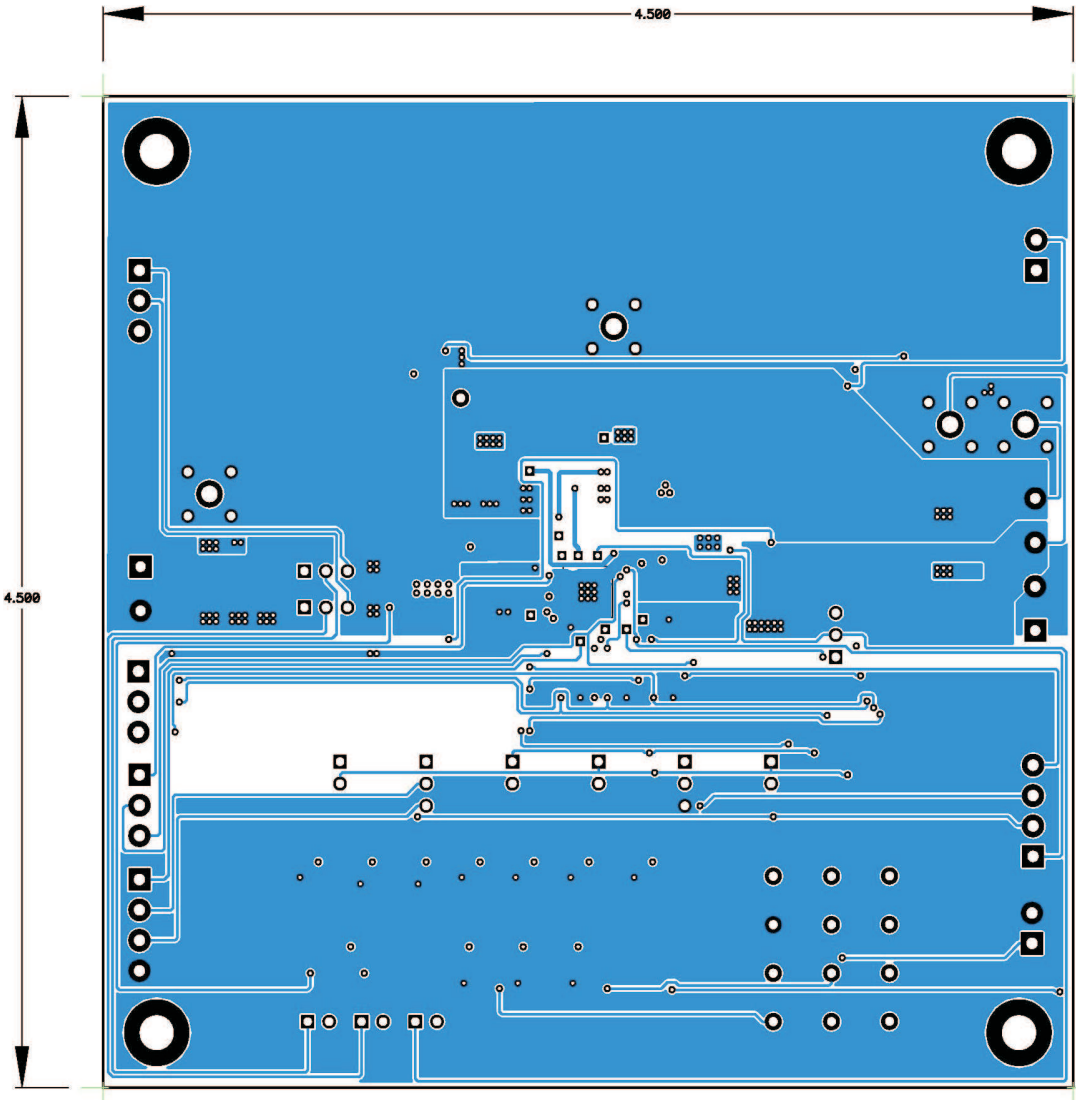


Figure 5. Third Layer

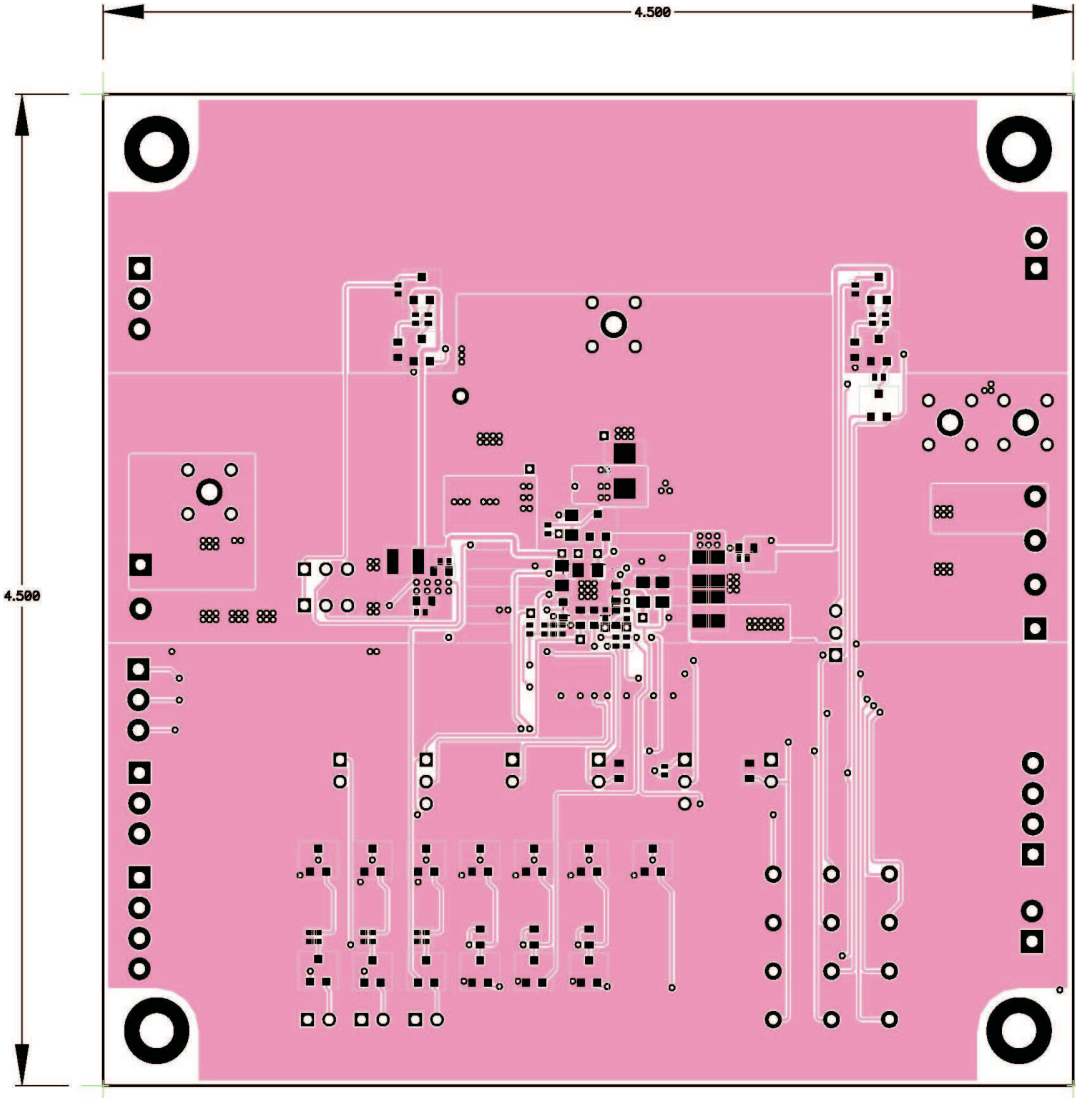


Figure 6. Bottom Layer

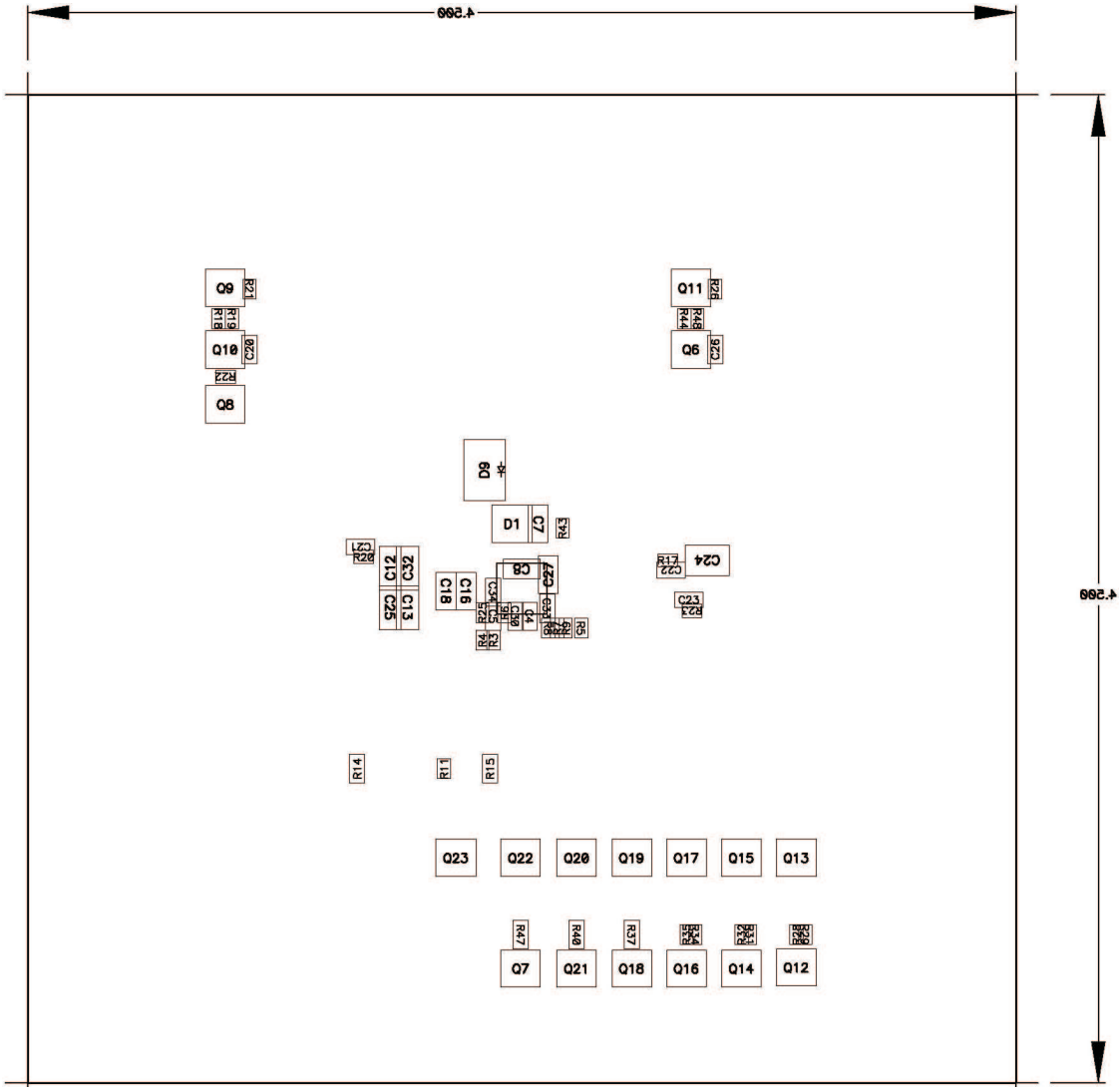


Figure 7. Bottom Assembly

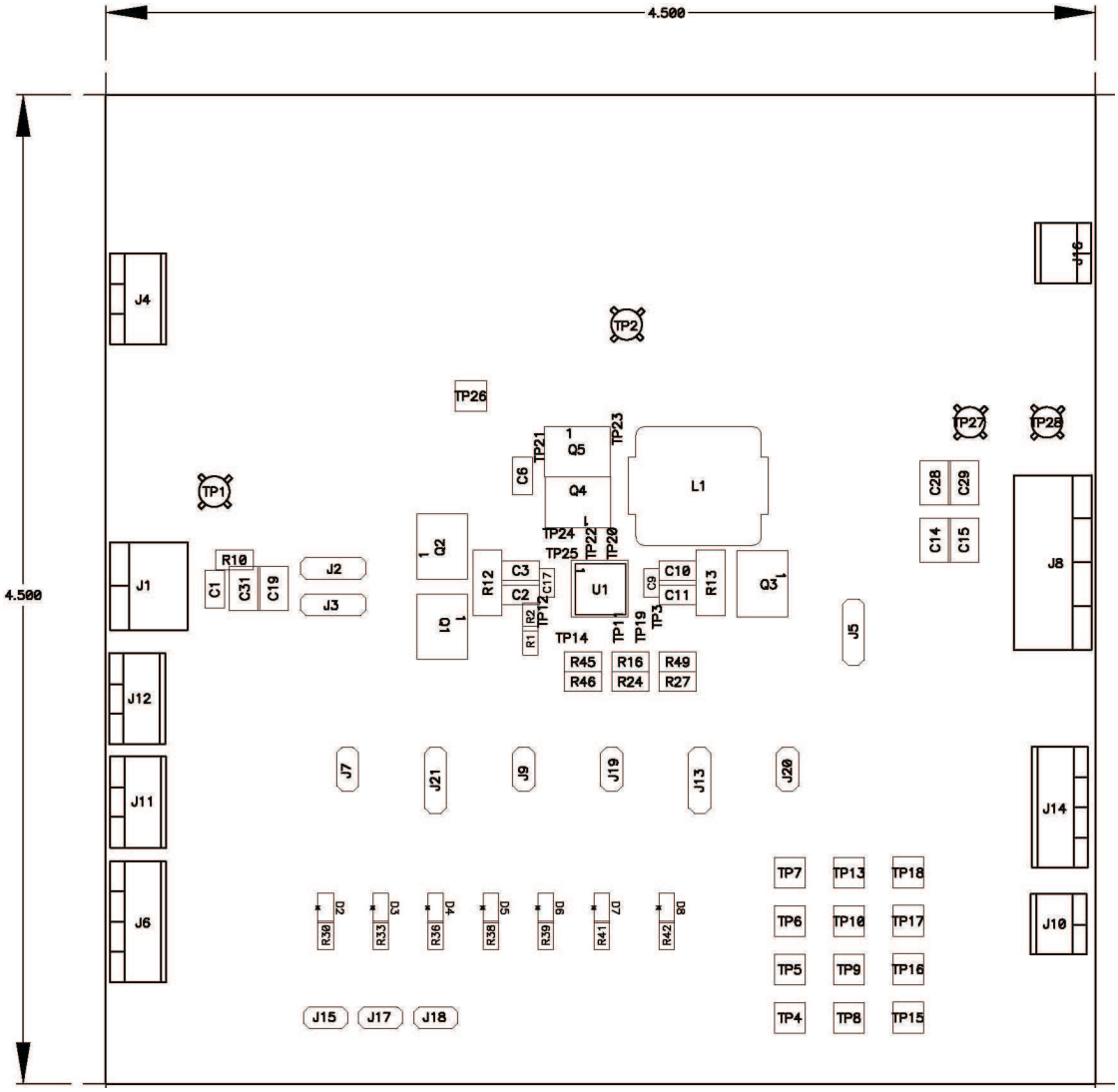
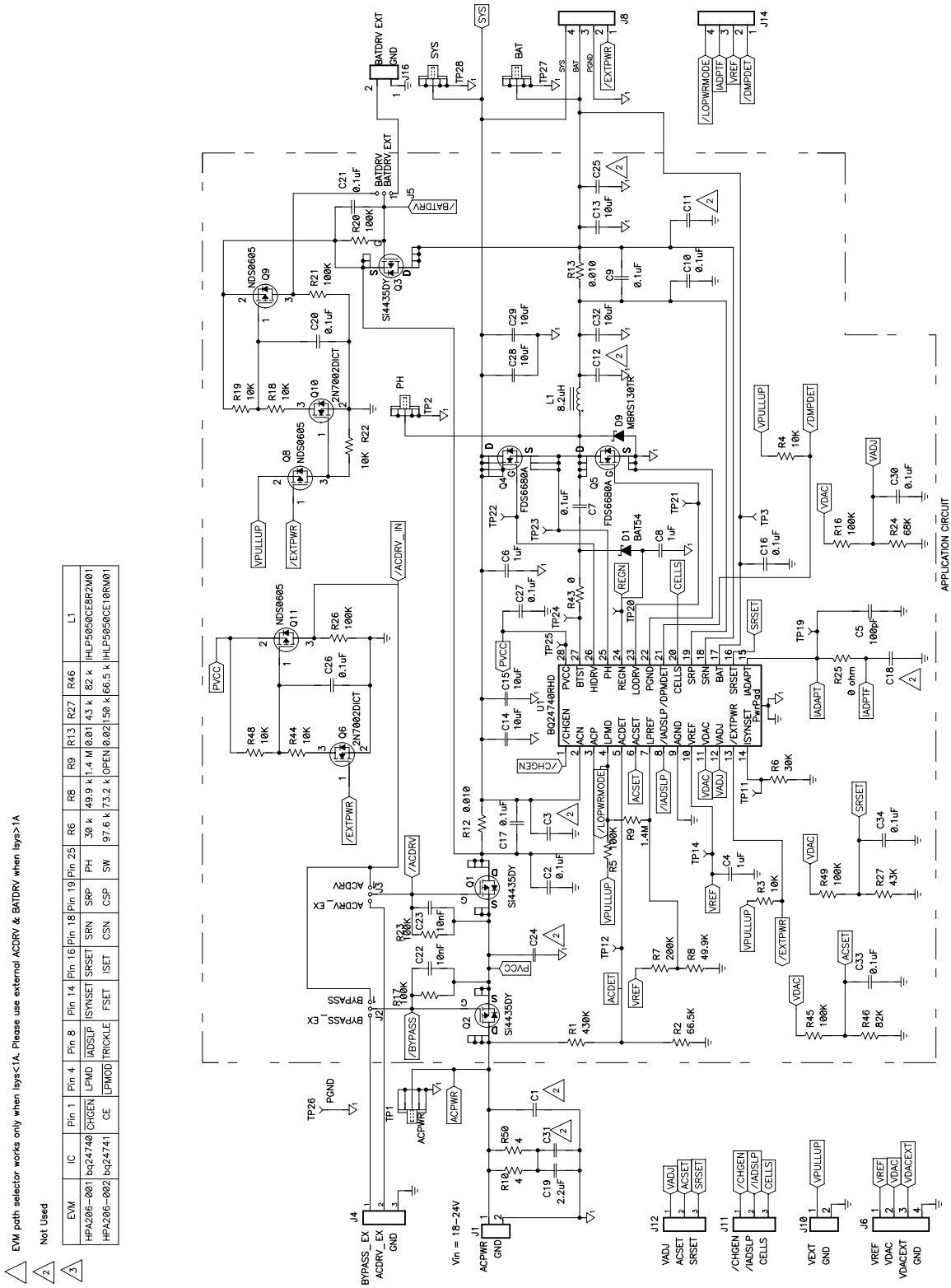
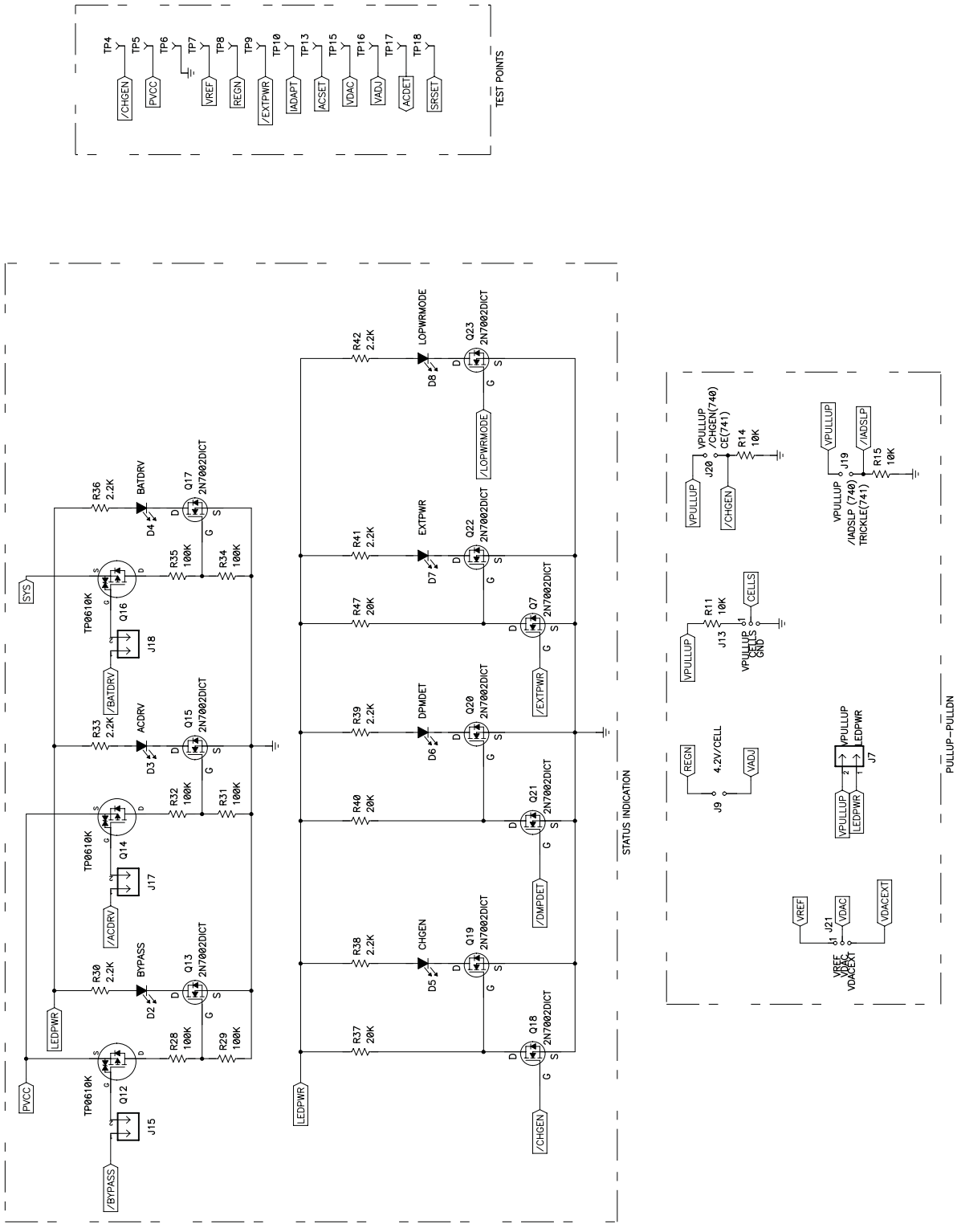


Figure 8. Top Assembly

4.3 Schematics



EVM	IC	Pin 1	Pin 4	Pin 8	Pin 14	Pin 16	Pin 18	Pin 19	Pin 25	R6	R8	R9	R13	R27	R46	L1
HPA206–001	bq24740	CHGEN	LPMD	IADSLP	ISYNSET	SRSET	SRN	SRP	PH	30 k	49.9 k	1.4 M	0.01	43 k	82 k	IHLP5050CE8R2M01
HPA206–002	bq24741	CE	LPMOD	TRICKLE	FSET	ISET	CSN	CSP	SW	97.6 k	73.2 k	OPEN	0.02	150 k	66.5 k	IHLP5050CE10RM01


TEST POINTS
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP13
TP15
TP16
TP17
TP18
/CHGEN
PVCC
VREF
REGN
/EXTPWR
IADAPT
ACSET
VDAC
VADJ
/ACDET
SRSET
STATUS INDICATION
PULLUP–PULLDN
SYS
PVCC
LEDPWR
/BYPASS
/ACDRV
/BATDRV
/CHGEN
/DMPDET
/EXTPWR
/LOPWRMODE
BATDRV
ACDRV
BYPASS
EXTPWR
DPMDET
CHGEN
LOPWRMODE
TP0610K
2N7002DICT
VPULLUP
/CHGEN(740)
CE(741)
/IADSLP (740)
TRICKLE(741)
/IADSLP
4.2V/CELL
CELLS
GND
VREF
VDAC
VDACEXT

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